FPGA Prototyping

Author: A.S. Aslanyan

Introduction:
FPGA prototyping is a well-established technique for verifying the functionality and performance of application-specific IC's by porting their RTL to a field programmable gate array. It is being used more widely today because hardware complexity is increasing, as well as the amount of related firmware that needs hardware-software co-verification.

Objective:
The goal of the course is to study the basic principles and methods of FPGA prototyping. The FPGA Prototyping course will provide you with a hands-on introduction to Verilog synthesis and FPGA programming through a “learn by doing” approach. It also focuses on the study of principles of IC prototyping; hardware and software; design strategies and methods.

Class Hours:
The course duration is 64 hours, lectures volume is 32 hours and laboratory works are 32 hours.

Prerequisites:
The course program is compiled taking into account that the following skills had been studied in advance:

- Digital Integrated Circuits
- Hardware Description Languages

Reference Materials:
To study the course the necessary list of references is given below.

1. P. Chu Pong, “FPGA Prototyping by Verilog Examples”, Xilinx Spartan, 3rd version, 2008
2. S. Kilts, “Advanced FPGA Design Architecture, Implementation, and Optimization”, 2007
3. Spartan-3A/3AN FPGA Starter Kit Board User Guide, 2010

Lectures (32 hours):

Topic 1.1 (2 hours) – Introduction

- Introduction of the programmable logic devices: Field Programmable Gate Array (FPGA), Programmable Logic Device (PLD), FPGA manufacturers (Xilinx, Altera, Actel, Lattice Semiconductor, Atmel). FPGA applications. Adjoining devices. Instruments and software.

Topic 1.2 (6 hours) – The structure of FPGA

- FPGA general description. Defining a types of FPGA packages. FPGA architecture. FPGA internal hard coded modules (CLB, Block RAM, DCM), the meanings and usage of these modules. Learning a type of I/O modules, the field of usage as well as configuration principles of different I/O types.

Topic 1.3 (4 hours) – FPGA design flow

- Architecture design. Project design using Verilog Hardware Description Language (HDL). Learning a testing methodology and testbench design. RTL simulation, synthesizing, implementation, gate level simulation of design. Reusing of internal hard modules during design and implementation.

Topic 1.4 (6 hours) – Using Verilog HDL during design flow

- Digital logic design basics. Defining a state machine types, implementation mechanisms and encoding styles, RTL and gate level design.

Copyright © 2021 “ASEC Technology”
www.asectec.com

Topic 1.5 (4 hours) – Testing methodology

- Functional and gate level testing, SDF file description and usage.

Topic 1.6 (2 hours) – FPGA configuration

- Different types of FPGA configuration files. Generation of configuration file and its loading into FPGA.

Topic 1.7 (4 hours) – Structure of PCB with FPGA

- Devices used with FPGA on a single board, Overview and General structure of PCB, PCB Types and Layers Structure, PCB design flow and Steps.

Topic 1.8 (4 hours) – Real time onboard testing and bug fixes

- Devices required for real time onboard testing (Logic Analyzer, Digital Oscilloscope, Multimeter, etc).

Laboratory Works (32 hours):

Topic 2.1 Introducing the FPGA development board (2 hours)
Topic 2.2 Analysis of basic components of FPGA development board (2 hours)
Topic 2.3 Analysis of lab design (2 hours)
Topic 2.4 Subdivision of the project based on the functional units (2 hours)
Topic 2.5 Coding of functional units in Verilog HDL (12 hours)
Topic 2.6 Designing a top module (2 hours)
Topic 2.7 Synthesis and implementation (6 hours)
Topic 2.8 Generating and loading the project into FPGA (1 hour)
Topic 2.9 Measuring signals in test points (1 hour)
Topic 2.10 Analysis of the results. (2 hours)

Copyright © 2021 “ASEC Technology”
www.asectec.com