Verilog HDL

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Introduction:
The popularity of Verilog HDL usage for all hardware applications rapidly increases. Our Verilog course modules uses the IEEE 1364 -2001 standard, offering everything you need to get started.

Objective:
The goal of the course is to teach you how to take advantage of this powerful and concise language for hardware modeling, design verification, and RTL synthesis.
The hands-on exercises in this training are designed to balance practical language application with ongoing learning and familiarization. Each exercise requires the students to prepare a fully functional code for the intended module or hardware description.

Class Hours:
The course duration is 34 hours, lectures volume is 20 hours and laboratory works are 14 hours.

Prerequisites:
The course program is compiled taking into account that the following skills had been studied in advance:

- Digital Integrated Circuits

Reference Materials:
To study the course the necessary list of references is given below.

1. Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, 2003
2. Thomas D.E./Moorby P.R. “The Verilog Hardware Description Language”, 5-th edition, 2002
3. Deepak Kumar Tala, “Verilog Tutorial”

Lectures (20 hours):

Topic 1.1 (2 hours) – Introduction

- Introduction of the Hardware Description Languages. Field of applications. Overview of CAD tools and design flow.

Topic 1.2 (6 hours) – Getting started with Verilog HDL

- Verilog HDL concepts
- Modules & Ports
- Verilog Operators & Expressions
- Data-Flow level coding

Topic 1.3 (6 hours) – FPGA / RTL optimized Verilog coding

- Behavioral level coding
- Advanced process statements
- FSM coding in Verilog
- Targeting FPGAs/Xilinx

Topic 1.4 (6 hours) – Behavioral coding in Verilog

- Testbenches in Verilog
- Verilog Tasks & Functions
- Timing simulation for post place & layout netlist

Laboratory Works (14 hours):

Topic 2.1	Coding and simulation of Decoder and Encoders (2 hours)
Topic 2.2	Coding and simulation of Mux (2 hours)
Topic 2.3	Coding and simulation of Flip Flop and Latches (2 hours)
Topic 2.4	Coding and simulation of Counters and LFSR (2 hours)
Topic 2.5	Coding and simulation of Parity and CRC (2 hours)
Topic 2.6	Coding and simulation of Memories (2 hours)
Topic 2.7	Coding and simulation of Verilog UART Model (2 hours)